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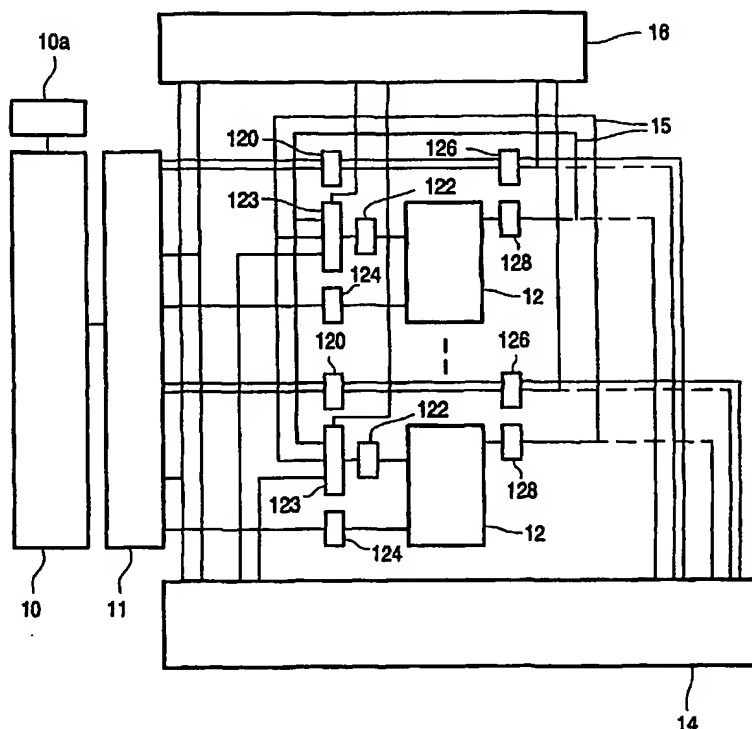
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(54) Title: PIPELINED INSTRUCTION PROCESSOR WITH DATA BYPASSING



(57) Abstract: An instruction processing device has a of pipe-line stage with a functional unit for executing a command from an instruction. A first register unit is coupled to the functional unit for storing a result of execution of the command when the command has reached a first one of the pipeline stages, and for supplying bypass operand data to the functional unit. A register file is coupled to the functional unit for storing the result when the command has reached a second one of the pipeline stages, downstream from the first one of the pipeline stages, and for supplying operand data to the functional unit. A disable circuit is coupled to selectively disable storing of the results in the register file under control of the instructions.

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KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

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## B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 145 074 A (ASATO ET AL) 7 November 2000 (2000-11-07)  the whole document	1, 2, 4-6, 9-11, 13, 14
X	EP 1 199 629 A (STMICROELECTRONICS S.R.L.) 24 April 2002 (2002-04-24) abstract paragraph '0052! - paragraph '0060! claims 1-3; figure 2	1, 10, 13
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P, A	US 2003/212915 A1 (LUICK DAVID A) 13 November 2003 (2003-11-13)	



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Information on patent family members

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